WE CLAIM:

1. A level-down level conversion circuit, comprising:

differential input means for receiving complementary input signals of a first amplitude; and

means for outputting a signal having a second amplitude that is smaller than said first amplitude.

2. A level-down level conversion circuit, comprising:

first and second field-effect transistors respectively arranged to receive complementary input signals of a first amplitude; and

third and fourth field-effect transistors of polarity opposite to that of the first and second field-effect transistors;

wherein the sources of the first and second field-effect transistors are coupled to a first voltage level, the sources of the third and fourth field-effect transistors are coupled to a second voltage level, and the drain of the second field-effect transistor and the gate of the third field-effect transistors are coupled to an output node of the level-down level conversion circuit.

3. A level-down level conversion circuit as claimed in claim 2, wherein the ground level of said complementary input signals fluctuates more than (the threshold voltage of said first and second field-effect transistors) (one-half of the power supply voltage of the level conversion circuit).

4. A level-down level conversion circuit, comprising:

a first NMOS transistor receiving one of a pair of differential input signals at a gate thereof and having a source connected to a first voltage;

a second NMOS transistor receiving the other of said pair of differential input signals at a gate thereof and having a source connected to the first voltage;

a first PMOS transistor having a source connected to a second voltage, a drain connected to a drain of the first NMOS transistor, and a gate connected to the drain of the second NMOS transistor; and

a second PMOS transistor having a source connected to the second voltage, a drain connected to the drain of the second NMOS transistor, and a gate connected to the drain of the first NMOS transistor.

5. A level-down level conversion circuit according to claim 4, wherein the first and second PMOS transistors have gate oxide layers that are thinner than gate oxide layers of the first and second NMOS transistors.

6. A level-down level conversion circuit according to claim 4, wherein the first and second PMOS transistors have lower thresholds than the first and second NMOS transistors.

7. A level-down level conversion circuit as claimed in claim 4, further comprising an inverter coupled to the drain of the second NMOS transistor.

8. In a semiconductor integrated circuit device having a plurality of circuit blocks, at least two of said circuit blocks having different respective operating voltages, the improvement comprising a level-down level conversion circuit for converting the level of a signal received from a high-voltage circuit block for supply to a low-voltage circuit block;

wherein said level-down level conversion circuit includes differential input means for receiving complementary input signals of a first amplitude, and means for outputting a signal having a second amplitude that is lower than said first amplitude.

9. A semiconductor integrated circuit device, comprising:

a level-up level conversion circuit;

an output buffer circuit including a first PMOS transistor having its source connected to a first voltage and a first NMOS transistor having its drain connected to a drain of the first PMOS transistor and its source connected to a reference voltage, in which input signals are inputted into gates of the first PMOS transistor and the first NMOS transistor and the drain of the first NMOS transistor is used as an output, wherein the output buffer circuit receives the signal output by the level conversion circuit and

between the level-up level conversion circuit and the output buffer circuit, a first inverter circuit connected to

the gate of the first PMOS transistor and a second inverter circuit connected to the gate of the first NMOS transistor, a second NMOS transistor having a drain connected to the input of the first inverter circuit, a source connected to the reference voltage, and a gate connected to the output of the second inverter circuit, and a second PMOS transistor having a drain connected to the input of the second inverter circuit, a source connected to the first voltage, and a gate connected to the output of the first inverter circuit.

10. A semiconductor integrated circuit device as claimed in claim 9, wherein when the first voltage is high at the same time that the input signal is low, substantially no current flows between the first voltage and the reference voltage of the output buffer circuit.

11. A semiconductor integrated circuit device, comprising:

a level-up level conversion circuit;

an output buffer circuit including a first PMOS transistor having its source connected to a first voltage and a first NMOS transistor having its drain connected to a drain of the first PMOS transistor and its source connected to a reference voltage, in which input signals are inputted into gates of the first PMOS transistor and the first NMOS transistor and the drain of the first NMOS transistor is used as an output, wherein the output buffer circuit receives the signal output by the level-up level conversion circuit; and

means for preventing a current from flowing through the output buffer circuit when only one of said first PMOS transistor and said first NMOS transistor is on.

12. A level-up level conversion circuit, comprising:

first and second field-effect transistors arranged to receive complementary input signals of a first amplitude, wherein the sources of the first and second field-effect transistors are coupled to a first voltage level;

third and fourth field-effect transistors arranged to receive said complementary input signals of said first amplitude, the first and second field-effect transistors being of opposite polarity to that of the third and fourth field-effect transistors, wherein the drains of the third and fourth field-effect transistors are respectively coupled to the drains of the first and second field-effect transistors;

fifth and sixth field-effect transistors of mutually opposite polarities, wherein the gate of the fifth field-effect transistor is coupled to the drain of the fourth field-effect transistor and to an output node of the level conversion circuit, the gate of the sixth field-effect transistor is coupled to the drain of the third field-effect transistor, and the sources of the third and fourth field-effect transistors are respectively coupled to the drains of the fifth and sixth field-effect transistors; and

a seventh field-effect transistor having a source connected to a second voltage level, a gate connected to

ground, and a drain connected to the sources of the fifth and sixth field-effect transistors.

13. A level-up level conversion circuit, comprising:

a first NMOS transistor receiving one of a pair of differential input signals at a gate thereof and having a source connected to a first voltage;

a second NMOS transistor receiving the other of said pair of differential input signals at a gate thereof and having a source connected to the first voltage;

a first PMOS transistor receiving said one of said pair of differential input signals at a gate thereof and having a drain connected to the drain of the first NMOS transistor;

a second PMOS transistor receiving said other of said pair of differential input signals at a gate thereof and having a drain connected to the drain of the second NMOS transistor;

third and fourth PMOS transistors respectively having drains connected to the sources of said first and second PMOS transistors; and

a fifth PMOS transistor having a source connected to a second voltage, a gate connected to ground, and a drain connected to the sources of said third and fourth PMOS transistors.

14. A level-up level conversion circuit as claimed in claim 13, further comprising an inverter coupled to the drain of the second NMOS transistor.

15. A level-up level conversion circuit, comprising:

a first NMOS transistor receiving one of a pair of differential input signals at a gate thereof and having a source connected to a first voltage;

a second NMOS transistor receiving the other of said pair of differential input signals at a gate thereof and having a source connected to the first voltage;

a first PMOS transistor receiving said one of said pair of differential input signals at a gate thereof and having a drain connected to the drain of the first NMOS transistor;

a second PMOS transistor receiving said other of said pair of differential input signals at a gate thereof and having a drain connected to the drain of the second NMOS transistor;

third and fourth PMOS transistors respectively having drains connected to the sources of said first and second PMOS transistors; and

an inverter coupled to the drain of the second NMOS transistor.

16. A level-up level conversion circuit, comprising:

first and second NMOS transistors having respective sources coupled to a first voltage;

a first PMOS transistor having a drain coupled to the drains of the first and second NMOS transistors;

a second PMOS transistor having a drain coupled to the source of the first PMOS transistor;

wherein the gates of said first NMOS transistor and said second PMOS transistor are arranged to receive one of a first pair of complementary input signals, and wherein the gates of the second NMOS transistor and the first PMOS transistor are arranged to receive one of a second pair of complementary input signals;

third and fourth PMOS transistors;

a third NMOS transistor having a drain coupled to the drains of the third and fourth PMOS transistors;

a fourth NMOS transistor having a drain coupled to the source of the third NMOS transistor and a source coupled to the first voltage;

wherein the gates of the third PMOS transistor and the third NMOS transistor are arranged to receive the other of the first pair of complementary input signals, and wherein the gates of the fourth PMOS transistor and the fourth NMOS transistor are arranged to receive the other of the second pair of complementary input signals;

a fifth PMOS transistor having a source coupled to a second voltage, a gate coupled to the drains of the third and fourth PMOS transistors, and a drain coupled to the source of the second PMOS transistor; and

a sixth PMOS transistor having a source coupled to the second voltage, a gate coupled to the drains of the first and second NMOS transistors, and a drain coupled to the sources of the third and fourth PMOS transistors.

17. A level-up level conversion circuit as claimed in claim 16, further comprising an inverter coupled to the drain of the third NMOS transistor.

18. A level-up level conversion circuit, comprising:

a NOR circuit arranged to receive at least two input signals;

a NAND circuit arranged to receive the complements of said at least two input signals; and

means functionally coupling said NOR circuit and said NAND circuit such that said level-up level conversion circuit provides an output signal that is the logical OR of said at least two input signals, said output signal having an amplitude that is larger than that of said at least two input signals when any of said at least two input signals becomes high.

19. A level-up level conversion circuit, comprising:

a logic circuit arranged to receive at least two input signals;

a NAND circuit arranged to receive the complements of said at least two input signals; and

means functionally coupling said logic circuit and said NAND circuit such that said level-up level conversion circuit performs the inverse of the logical operation performed by said logic circuit on said at least two input signals, said output signal having an amplitude that is larger than that of

said at least two input signals when any of said at least two input signals becomes high.

20. A level conversion circuit, comprising:

first and second NMOS transistors having respective sources coupled to a first voltage;

a first PMOS transistor having a drain coupled to the drains of the first and second NMOS transistors;

a second PMOS transistor having a drain coupled to the source of the first PMOS transistor;

wherein the gates of said first NMOS transistor and said second PMOS transistor are arranged to receive one of a first pair of complementary input signals, and wherein the gates of the second NMOS transistor and the first PMOS transistor are arranged to receive one of a second pair of complementary input signals;

third and fourth PMOS transistors;

a third NMOS transistor having a drain coupled to the drains of the third and fourth PMOS transistors;

a fourth NMOS transistor having a drain coupled to the source of the third NMOS transistor and a source coupled to the first voltage;

wherein the gates of the third PMOS transistor and the third NMOS transistor are arranged to receive the other of the first pair of complementary input signals, and wherein the gates of the fourth PMOS transistor and the fourth NMOS

transistor are arranged to receive the other of the second pair of complementary input signals;

a fifth PMOS transistor having a source coupled to a second voltage, a gate coupled to the drains of the third and fourth PMOS transistors, and a drain coupled to the source of the second PMOS transistor;

a sixth PMOS transistor having a source coupled to the second voltage, a gate coupled to the drains of the first and second NMOS transistors, and a drain coupled to the sources of the third and fourth PMOS transistors; and

an inverter arranged to receive said one of the second pair of complementary input signals and to output said other of the second pair of complementary input signals to the gates of the fourth PMOS transistor and the fourth NMOS transistor.

21. A level conversion circuit as claimed in claim 20, wherein when said one of the second pair of complementary input signals is low, the output of the level conversion circuit is always high.

22. A level conversion circuit as claimed in claim 20, wherein when said one of the second pair of complementary input signals is low, no through-current flows from said second voltage to said first voltage.

23. A level conversion circuit as claimed in claim 20, wherein the second NMOS transistor, the second PMOS transistor, the fourth NMOS transistor, and the fourth PMOS transistor have gate lengths that are smaller than the gate

lengths of the first NMOS transistor, the first PMOS transistor, the third NMOS transistor, and the third PMOS transistor.

24. A level conversion circuit as claimed in claim 20, wherein when said one of the second pair of complementary input signals is high, the output of the level conversion circuit is always low.

25. A level conversion circuit, comprising:

a first NMOS transistor arranged to receive a first input signal on a gate thereof;

a second NMOs transistor arranged to receive the complement of said first input signal on a gate thereof;

a first PMOS transistor arranged to receive said first input signal on a gate thereof, said first PMOS transistor having a drain coupled to the drain of said first NMOS transistor;

a second PMOS transistor arranged to receive said complement of said first input signal on a gate thereof, said second PMOS transistor having a drain coupled to the drain of said second NMOS transistor;

a third PMOS transistor having a source connected to a first voltage, a gate connected to the drains of said second NMOS transistor and second PMOS transistor, and a drain connected to the source of said first PMOS transistor;

a fourth PMOS transistor having a source connected to said first voltage, a gate connected to the drains of said

first NMOS transistor and said first PMOS transistor, and a drain connected to the source of said second PMOS transistor;

a third NMOS transistor having a source coupled to a second voltage, a gate arranged to receive a second input signal, and a drain connected to the sources of the first and second NMOS transistors; and

a fifth PMOS transistor having a source coupled to said first voltage, a gate connected to the gate of said third NMOS transistor, and a drain connected to the drains of said second NMOS transistor and said second PMOS transistor.

26. A level conversion circuit, comprising:

a first NMOS transistor having a source coupled to a first voltage, and a gate arranged to receive a first input signal;

a second NMOS transistor having a source coupled to said first voltage, and a gate arranged to receive the complement of said first input signal;

a first PMOS transistor arranged to receive said first input signal on a gate thereof, said first PMOS transistor having a drain coupled to the drain of said first NMOS transistor;

a second PMOS transistor arranged to receive said complement of said first input signal on a gate thereof, said second PMOS transistor having a drain coupled to the drain of said second NMOS transistor;

a third PMOS transistor having a gate connected to the drains of said second NMOS transistor and second PMOS transistor, and a drain connected to the source of said first PMOS transistor;

a fourth PMOS transistor having a gate connected to the drains of said first NMOS transistor and said first PMOS transistor, and a drain connected to the source of said second PMOS transistor;

a fifth PMOS transistor having a source coupled to a second voltage, a gate arranged to receive a second input signal, and a drain connected to the sources of the third and fourth PMOS transistors; and

a third NMOS transistor having a source connected to ground, a gate connected to the gate of said fifth PMOS transistor, and a drain connected to the drains of said second NMOS transistor and said second PMOS transistor.

27. A circuit block, comprising:

a level conversion circuit including:

first and second NMOS transistors having respective sources coupled to a first voltage;

a first PMOS transistor having a drain coupled to the drains of the first and second NMOS transistors;

a second PMOS transistor having a drain coupled to the source of the first PMOS transistor;

wherein the gates of said first NMOS transistor and said second PMOS transistor are arranged to receive one

of a first pair of complementary input signals, and wherein the gates of the second NMOS transistor and the first PMOS transistor are arranged to receive one of a second pair of complementary input signals;

third and fourth PMOS transistors;

a third NMOS transistor having a drain coupled to the drains of the third and fourth PMOS transistors;

a fourth NMOS transistor having a drain coupled to the source of the third NMOS transistor and a source coupled to the first voltage;

wherein the gates of the third PMOS transistor and the third NMOS transistor are arranged to receive the other of the first pair of complementary input signals, and wherein the gates of the fourth PMOS transistor and the fourth NMOS transistor are arranged to receive the other of the second pair of complementary input signals;

a fifth PMOS transistor having a source coupled to a second voltage, a gate coupled to the drains of the third and fourth PMOS transistors, and a drain coupled to the source of the second PMOS transistor;

a sixth PMOS transistor having a source coupled to the second voltage, a gate coupled to the drains of the first and second NMOS transistors, and a drain coupled to the sources of the third and fourth PMOS transistors; and

an inverter arranged to receive said one of the second pair of complementary input signals and to output

said other of the second pair of complementary input signals to the gates of the fourth PMOS transistor and the fourth NMOS transistor; and

a latch arranged to receive and hold the output level of the level conversion circuit.

28. A circuit block as claimed in claim 27, wherein when said one of the second pair of complementary input signals is low, the output of the level conversion circuit is always high.

29. A circuit block as claimed in claim 27, wherein when said one of the second pair of complementary input signals is low, no through-current flows from said second voltage to said first voltage.

30. A circuit block as claimed in claim 27, wherein the second NMOS transistor, the second PMOS transistor, the fourth NMOS transistor, and the fourth PMOS transistor have gate lengths that are smaller than the gate lengths of the first NMOS transistor, the first PMOS transistor, the third NMOS transistor, and the third PMOS transistor.

31. A circuit block as claimed in claim 27, wherein when said one of the second pair of complementary input signals is high, the output of the level conversion circuit is always low.

32. A circuit block, comprising:

a level conversion circuit including:

a first NMOS transistor arranged to receive a first input signal on a gate thereof;

a second NMOs transistor arranged to receive the complement of said first input signal on a gate thereof;

a first PMOS transistor arranged to receive said first input signal on a gate thereof, said first PMOS transistor having a drain coupled to the drain of said first NMOS transistor;

a second PMOS transistor arranged to receive said complement of said first input signal on a gate thereof, said second PMOS transistor having a drain coupled to the drain of said second NMOS transistor;

a third PMOS transistor having a source connected to a first voltage, a gate connected to the drains of said second NMOS transistor and second PMOS transistor, and a drain connected to the source of said first PMOS transistor;

a fourth PMOS transistor having a source connected to said first voltage, a gate connected to the drains of said first NMOS transistor and said first PMOS transistor, and a drain connected to the source of said second PMOS transistor;

a third NMOS transistor having a source coupled to a second voltage, a gate arranged to receive a second input signal, and a drain connected to the sources of the first and second NMOS transistors; and

a fifth PMOS transistor having a source coupled to said first voltage, a gate connected to the gate of said third NMOS transistor, and a drain connected to the drains of said second NMOS transistor and said second PMOS transistor; and

a latch arranged to receive and hold the output level of the level conversion circuit.

33. A circuit block, comprising:

a level conversion circuit including:

a first NMOS transistor having a source coupled to a first voltage, and a gate arranged to receive a first input signal;

a second NMOS transistor having a source coupled to said first voltage, and a gate arranged to receive the complement of said first input signal;

a first PMOS transistor arranged to receive said first input signal on a gate thereof, said first PMOS transistor having a drain coupled to the drain of said first NMOS transistor;

a second PMOS transistor arranged to receive said complement of said first input signal on a gate thereof, said second PMOS transistor having a drain coupled to the drain of said second NMOS transistor;

a third PMOS transistor having a gate connected to the drains of said second NMOS transistor and second PMOS

transistor, and a drain connected to the source of said first PMOS transistor;

a fourth PMOS transistor having a gate connected to the drains of said first NMOS transistor and said first PMOS transistor, and a drain connected to the source of said second PMOS transistor;

a fifth PMOS transistor having a source coupled to a second voltage, a gate arranged to receive a second input signal, and a drain connected to the sources of the third and fourth PMOS transistors; and

a third NMOS transistor having a source connected to ground, a gate connected to the gate of said fifth PMOS transistor, and a drain connected to the drains of said second NMOS transistor and said second PMOS transistor; and

a latch arranged to receive and hold the output level of the level conversion circuit.

34. In a semiconductor integrated circuit device having a plurality of circuit blocks, at least two of said circuit blocks having different respective operating voltages, the improvement comprising a level-up level conversion circuit for converting the level of a signal received from a low-voltage circuit block for supply to a high-voltage circuit block;

wherein said level-up level conversion circuit includes:

first and second NMOS transistors having respective sources coupled to a first voltage;

a first PMOS transistor having a drain coupled to the drains of the first and second NMOS transistors;

a second PMOS transistor having a drain coupled to the source of the first PMOS transistor;

wherein the gates of said first NMOS transistor and said second PMOS transistor are arranged to receive one of a first pair of complementary input signals, and wherein the gates of the second NMOS transistor and the first PMOS transistor are arranged to receive one of a second pair of complementary input signals;

third and fourth PMOS transistors;

a third NMOS transistor having a drain coupled to the drains of the third and fourth PMOS transistors;

a fourth NMOS transistor having a drain coupled to the source of the third NMOS transistor and a source coupled to the first voltage;

wherein the gates of the third PMOS transistor and the third NMOS transistor are arranged to receive the other of the first pair of complementary input signals, and wherein the gates of the fourth PMOS transistor and the fourth NMOS transistor are arranged to receive the other of the second pair of complementary input signals;

a fifth PMOS transistor having a source coupled to a second voltage, a gate coupled to the drains of the third and fourth PMOS transistors, and a drain coupled to the source of the second PMOS transistor;

a sixth PMOS transistor having a source coupled to the second voltage, a gate coupled to the drains of the first and second NMOS transistors, and a drain coupled to the sources of the third and fourth PMOS transistors; and

an inverter arranged to receive said one of the second pair of complementary input signals and to output said other of the second pair of complementary input signals to the gates of the fourth PMOS transistor and the fourth NMOS transistor.

35. A semiconductor integrated circuit device as claimed in claim 34, wherein when said one of the second pair of complementary input signals is low, the output of the level conversion circuit is always high.

36. A semiconductor integrated circuit device as claimed in claim 34, wherein when said one of the second pair of complementary input signals is low, no through-current flows from said second voltage to said first voltage.

37. A semiconductor integrated circuit device as claimed in claim 34, wherein the second NMOS transistor, the second PMOS transistor, the fourth NMOS transistor, and the fourth PMOS transistor have gate lengths that are smaller than the gate lengths of the first NMOS transistor, the first PMOS transistor, the third NMOS transistor, and the third PMOS transistor.

38. A semiconductor integrated circuit device as claimed in claim 34, wherein when said one of the second pair of

complementary input signals is high, the output of the level conversion circuit is always low.

39. In a semiconductor integrated circuit device having a plurality of circuit blocks, at least two of said circuit blocks having different respective operating voltages, the improvement comprising one of said circuit blocks having a level-up level conversion circuit for converting the level of a signal received from a low-voltage circuit block for supply to a high-voltage circuit block, and a latch arranged to receive and hold the output level of the level-up level conversion circuit;

wherein said level-up level conversion circuit includes:

a first NMOS transistor arranged to receive a first input signal on a gate thereof;

a second NMOs transistor arranged to receive the complement of said first input signal on a gate thereof;

a first PMOS transistor arranged to receive said first input signal on a gate thereof, said first PMOS transistor having a drain coupled to the drain of said first NMOS transistor;

a second PMOS transistor arranged to receive said complement of said first input signal on a gate thereof, said second PMOS transistor having a drain coupled to the drain of said second NMOS transistor;

a third PMOS transistor having a source connected to a first voltage, a gate connected to the drains of said

second NMOS transistor and second PMOS transistor, and a drain connected to the source of said first PMOS transistor;

a fourth PMOS transistor having a source connected to said first voltage, a gate connected to the drains of said first NMOS transistor and said first PMOS transistor, and a drain connected to the source of said second PMOS transistor;

a third NMOS transistor having a source coupled to a second voltage, a gate arranged to receive a second input signal, and a drain connected to the sources of the first and second NMOS transistors; and

a fifth PMOS transistor having a source coupled to said first voltage, a gate connected to the gate of said third NMOS transistor, and a drain connected to the drains of said second NMOS transistor and said second PMOS transistor.

40. In a semiconductor integrated circuit device having a plurality of circuit blocks, at least two of said circuit blocks having different respective operating voltages, the improvement comprising one of said circuit blocks having a level-up level conversion circuit for converting the level of a signal received from a low-voltage circuit block for supply to a high-voltage circuit block, and a latch arranged to receive and hold the output level of the level-up level conversion circuit;

wherein said level-up level conversion circuit includes:

a first NMOS transistor having a source coupled to a first voltage, and a gate arranged to receive a first input signal;

a second NMOS transistor having a source coupled to said first voltage, and a gate arranged to receive the complement of said first input signal;

a first PMOS transistor arranged to receive said first input signal on a gate thereof, said first PMOS transistor having a drain coupled to the drain of said first NMOS transistor;

a second PMOS transistor arranged to receive said complement of said first input signal on a gate thereof, said second PMOS transistor having a drain coupled to the drain of said second NMOS transistor;

a third PMOS transistor having a gate connected to the drains of said second NMOS transistor and second PMOS transistor, and a drain connected to the source of said first PMOS transistor;

a fourth PMOS transistor having a gate connected to the drains of said first NMOS transistor and said first PMOS transistor, and a drain connected to the source of said second PMOS transistor;

a fifth PMOS transistor having a source coupled to a second voltage, a gate arranged to receive a second input

signal, and a drain connected to the sources of the third and fourth PMOS transistors; and

a third NMOS transistor having a source connected to ground, a gate connected to the gate of said fifth PMOS transistor, and a drain connected to the drains of said second NMOS transistor and said second PMOS transistor.